BOX PATENT
Attorney Docket No. 24810

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Ralf KOERNLE
Juergen MOTZER
Albert WÖHRLE

Serial No.: Not Yet Assigned

Filed: November 15, 2001

For: **CIRCUIT CONFIGURATION FOR THE VOLTAGE SUPPLY OF A TWO-WIRE SENSOR**

PRELIMINARY AMENDMENT

The Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examining on the merits and calculating the filing fee for the above-captioned patent application filed herewith, please amend the application as follows:

IN THE CLAIMS

Please amend claims 3 and 5 as per attached with this preliminary amendment. Pursuant to the new rules implementing the AIPA, a clean copy of the amended claims is attached along with a marked-up copy of the claims indicating the proposed claims amendments.

REMARKS

The claims have been amended to clarify the subject matter and remove multiple dependencies. The amendments and newly added claims do not add any new matter within the meaning of 35 U.S.C. §132.

Early action on the merits is earnestly solicited.

Respectfully submitted,

NATH & ASSOCIATES PLLC

By: [signature]

Gary M. Nath
Registration No. 26,965
Customer No. 20529

Date: November 15, 2001

NATH & ASSOCIATES PLLC
1030 15th Street, NW - 6th Floor
Washington, D.C. 20005
GMN/ls:24810:AMENDpreml

CLEAN COPY OF CLAIMS AS AMENDED:

(Amended) 3. Circuit configuration as defined in Claim 1, characterized in that a pole of the supply voltage source (U) is connected to an input of two-wire sensor (S) via a HART® resistor (RH), the drain source path of a field effect transistor (T1), and the current-limiting resistor (R1), the other input of which sensor is connected to the other pole of the supply voltage source (U) via the second connection line (V2) that the HART® resistor (RH), the drain source path of the field effect transistor (T1) and the current-limiting resistor (R1) are positioned in the first connection line (V1), that the source electrode of the field effect transistor (T1) is connected to the second connection line (V2) via a series circuit comprising a first and second limiting diode (D1, D2), that a first resistor (R4) is positioned parallel to the second limiting diode (D2), that the joint node of the second limiting diode (D2) and the first resistor (R4) is connected to the base of a transistor (T2), the collector of which is connected to the gate

electrode of field effect transistor (T1) via a second resistor (R3), and the emitter of which is connected to the second connection line (V2), and that the gate electrode of the field effect transistor (T1) is connected to the source electrode via a third resistor (R2).

(Amended) 5. Circuit configuration as defined in claim 4, characterized in that the series connected limiting diodes (D1 through D6) are oppositely poled.

MARKED UP COPY OF CLAIM AMENDMENTS:

(Amended) 3. Circuit configuration as defined in Claim 1 [or 2], characterized in that a pole of the supply voltage source (U) is connected to an input of two-wire sensor (S) via a HART® resistor (RH), the drain source path of a field effect transistor (T1), and the current-limiting resistor (R1), the other input of which sensor is connected to the other pole of the supply voltage source (U) via the second connection line (V2) that the HART® resistor (RH), the drain source path of the field effect transistor (T1) and the current-limiting resistor (R1) are positioned in the first connection line (V1), that the source electrode of the field effect transistor (T1) is connected to the second connection line (V2) via a series circuit comprising a first and second limiting diode (D1, D2), that a first resistor (R4) is positioned parallel to the second limiting diode (D2), that the joint node of the second limiting diode (D2) and the first resistor (R4) is connected to the base of a transistor (T2), the collector of which is connected to the gate

electrode of field effect transistor (T1) via a second resistor (R3), and the emitter of which is connected to the second connection line (V2), and that the gate electrode of the field effect transistor (T1) is connected to the source electrode via a third resistor (R2).

(Amended) 5. Circuit configuration as defined in <u>claim 4</u> [one of the preceding claims], characterized in that the series connected limiting diodes (D1 through D6) are oppositely poled.